UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,478	06/01/2001	Valerie Jo Young	26152/11:2	9496

3528 7590 10/06/2004

STOEL RIVES LLP
900 SW FIFTH AVENUE
SUITE 2600
PORTLAND, OR 97204

EXAMINER	
PATEL, JAY P	
ART UNIT	**PAPER NUMBER**
2666	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,478	YOUNG ET AL.	
	Examiner	Art Unit	
	Jay P. Patel	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25-33* is/are allowed.

6)☒ Claim(s) *1,10 and 16-18* is/are rejected.

7)☒ Claim(s) *2-9,11-15 and 19-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/05/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is objected to because of the following: The signatures of the inventors are not present in the oath/declaration.

Appropriate correction is required.

Objections – Informalities

2. Figures 1 and 2 are objected to because of the following informalities: The description of the figures present in the specifications contains numerical references to the different components of the drawings; the figures themselves however, do not contain these numerical references. For example, on page 7 of the specification in the detailed description of figure 1, the applicant states "Figure 1 is a conceptual illustration of a known time-division multiplexing (TDM) circuit for transmitting data communications from a first host (100) of a digital circuit to a receiving terminal (106)" (page 7 lines 18 through 20). The numerical references 100 and 106 are not present in figure 1. On page 8 the applicant states "Referring to figure 2, the first waveform (200) illustrates the /CT_FRAME signal. The second signal in figure 2 labeled (202) illustrates the CT_C8 bit clock," (page 8 lines 21 and 22). The numerical references 200 and 202 are not present in figure 2.

Appropriate correction is required.

3. The specification is objected to because of the following informalities: In the second sentence of the seventh paragraph of the summary of invention section of the

specifications, the word "with" must be inserted between the words "charged" and "buffering". In the detailed descriptions of figures 2 and 3, the frame synch signal is specified to have a period of 125 milliseconds and the frame pulse is specified to occur every 125 milliseconds; figure 2 however shows this period as 125 microseconds. Appropriate correction is required.

4. Claims 2 through 9, 11 through 15, 17 through 24, 26 through 30, 32 and 33 objected to because of the following informalities: The above mentioned claims depend either on an independent or a dependent claim that specifies either a system, a bridge product or a method; therefore, the above mentioned claims must start with "the" instead of "a" or "an".

Appropriate correction is required.

Claim 24 is objected to because of the following informalities: Claim 24 should be written on the next line after the conclusion of claim 23 and not on the same line as claim 23.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 10,16-18 are rejected under 35 U.S.C 102(e) as being anticipated by Muhammad et al. (U. S. Patent 6,650,649 B1).

Regarding claim 1, the reference discloses a quad DS1/AAL1 SSI module (Figure 20 and column 45 lines 55 through 67 continued on column 46 lines 1 through 6). The reference discloses a multi-transport cell bus, which is connected to a cell formatter, which extracts the necessary data from the bus (column 46 lines 31 through 35). The cells referred to by the reference are timeslots that carry distinct channels. This embodiment in the reference anticipates the input port disclosed by the applicant. It is further disclosed that the quad DS1/AAL1 SSI module is a dual transport mode module; therefore, "it can be configured to work in either TDM mode or ATM AAL1 mode" (column 46 lines 9 through 12). Figure 18 in the reference, discloses a timing diagram for the multi-transport cell bus; therefore it is inherent that the data on the multi-transport cell bus is synchronized to a pulse signal (column 53 lines 10 through 16). It is also inherent from the reference that the disclose invention provides users with " voice, video, and data connections to other networks: (column 2 lines 6 through 9). The reference also discloses a receive buffer which copies the data from the cell formatter;

furthermore, the receiver buffer is static RAM. It is further disclosed that as the cells are copied, the cell formatter unpacks them in to DSOs as necessary with TDM buffering (column 47 lines 34 through 40). The cell formatter after further processing sends the data to the PCMIF Logic and through a PCM bus, sends the data to the ATM processor; the timing logic also receives timing information from the multi-transport cell bus via the cell formatter and then sends data to the ATM processor (column 47 lines 45 through 49 and line 52). ATM cells are also routed from the cell formatter to the ATM processor via the utopia bus (column 47 lines 1 through 6). The ATM processor sends the data to the T1/E1 framers through the combination of the above-mentioned buses. The combination of the above mentioned buses anticipate the parallel bus interface claimed by the applicant and the ATM processor anticipates the network processor claimed by the applicant.

6. In regards to claim 10, the reference discloses that traffic enters the T1/E1 framers and then data flows to the AALI SAR, which is a part of the ATM processor (column 47 lines 14 through 18). The combination of buses disclosed with regard to claim 1 anticipates the parallel bus interface claimed by the applicant in claim 10. The transmit buffer disclosed in the reference (Figure 20) anticipates the transmit component claimed by the applicant. The data from the transmit buffer flows in to the cell formatter where it is multiplexed onto the multi-transport cell bus (column 47 lines 18 through 22). The multi-transport cell bus disclosed in this context by the reference, anticipates the TDM output port claimed by the applicant. The timing diagram disclosed

by figure 18 of the reference, anticipates the frame synchronization claimed by the applicant.

7. In regards to claim 16, the claim is a combination of the limitations in claims 1 and 10. The reference discloses that the different types of service specific interface (SSI) are intended to be "used to interface with the multi-transport mode cell bus", as well as "to format traffic for transmission on the multi-transport mode cell bus" (column 45 lines 49 through 54). The reference anticipates the applicant's claim of an interface system that is bidirectional in which information can travel both ways. Furthermore, in regards to figure 21 of the reference, it is disclosed that data can travel in opposite direction as well (column 47 lines 14 through 18). Therefore all the disclosers from the prior art used to reject claims 1 and 10 are also pertinent to claim 16.

8. In regards to claims 17 and 18, the reference discloses a processing section within the quad DS1/AAL1 SSI module (column 45 line 60). It is inherent from figure 21 of the reference that the processing unit disclosed, anticipates the CPU claimed by the applicant. The processing unit is connected to the control logic, the cell formatter, and the ATM processor and the processing unit further contains a microprocessor and a message buffer. The control logic disclosed by the reference anticipates the applicants' claim for a control interface in claim 17 and a control register claimed in claim 18.

Allowable Subject Matter

9. Claims 2-9, 11-15 and 19-24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 25-33 allowed.

11. In regards to claim 25, the cited reference fails to disclose **a TDM bridge product with a time slot switch means mounted on the circuit board and coupled to the first input connector for controllably selecting at least one time slot of the TDM input data and providing the selected time slot of serial data to a local bus.** It is noted that the reference does disclose a cell formatter and a multi-transport cell bus. The reference discloses that the cell formatter listens to the configured timeslot from the multi-transport mode cell bus; however, it fails to disclose the means by which the process takes place and therefore, fails to disclose or render obvious the above underlined limitations as claimed.

12. In regards to claim 31, the cited reference fails to disclose a method for **providing a plurality of N + 1 memory banks, where N is a positive integer; storing a first frame of the series of bytes into a first one of the memory banks; storing each subsequent frame of the series of bytes into a next succeeding one of the memory banks, until N frames of data are stored in respective memory banks; storing a next subsequent frame of the series of bytes in the N+ Ith memory bank; and while storing said next subsequent frame of the series of bytes in the N+ Ith memory bank, concurrently unloading the first N frames of data from the first N**

memory banks into a processor; responsive to a next frame pulse signal, rotating the memory banks; and then repeating said steps of storing and unloading the series of data bytes in an ongoing fashion for continuous real-time operation; and concurrently, in the processor, encapsulating the wide words of data so as to form a series of data packets bearing the TDM data; and transmitting the series of data packets on to a packet switched network. It is noted that the reference does disclose receive, transmit and message buffers; however, it fails to disclose the means by which bytes of data are organized in the buffers and furthermore fails to disclose a successive process for loading and unloading bytes of data. Therefore, the reference fails to disclose or render obvious the above underlined limitations as claimed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jay P. Patel whose telephone number is (571) 272-3086. The examiner can normally be reached on M-F 9:00 am - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jay P. Patel
Examiner
Art Unit 2666

jpp
September 30, 2004

RICKY NGO
PRIMARY EXAMINER

10/01/04